REMARKS

The applicant notes with appreciation that the Office Action indicates that claims 4-6 and 13 would be allowable if written in independent form. Accordingly, independent claim 1 is amended above to include the limitations of former claim 4. New claim 33 is claim 5 rewritten in independent form. New claim 34 is claim 6 rewritten in independent form. Independent claim 10 is amended to include the limitations of former claim 13. Accordingly, it is believed that amended independent claim 1 and claims 2, 3, 7-9, and 30 dependent thereon are allowable, and amended independent claim 10 and claims 11, 12, 14-16, and 31 dependent thereon are allowable. Reconsideration of the rejection of claims 1-3, 7-12, 14-16, and 30-31 is respectfully requested. In addition, allowance of new independent claims 33-34 is respectfully requested.

Applicants further note that the non-final Office Action dated May 13, 2005 indicated that former claims 4-6 and 13 would be allowable if rewritten in independent form. New claim 35 includes the limitations of original claims 1 and 4. New claim 36 includes the limitations of original claims 1 and 5. New claim 37 includes the limitations of original claims 1 and 6. New claim 38 includes the limitations of original claims 10 and 13. Allowance of new claims 35-38 is respectfully requested.

Independent claim 23 is amended to clarify certain details of the present invention. Specifically, claim 23 is amended to clarify that an internal voltage generating circuit is coupled to a control signal generating circuit for receiving a control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated. Claim 23 is further amended to clarify that the internal voltage generating circuit comprises at least one of a first switching circuit that cuts off an external power voltage applied to the internal voltage generating circuit when a control signal is activated, a second switching circuit that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal is activated, and a third switching circuit including a CMOS transmission gate which transmits the

driving signal when the control signal is inactivated.

With regard to the rejection of amended independent claim 23, it is submitted that Morishita fails to teach or suggest an internal voltage generating circuit comprising at least one of a first switching circuit that cuts off an external power voltage applied to the internal voltage generating circuit when a control signal is activated, a second switching circuit that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal is activated, and a third switching circuit including a CMOS transmission gate which transmits a driving signal when the control signal is inactivated, as claimed in amended independent claim 23. Morishita discloses a comparator CMM that includes transistors N3, N4, N5, P7, and P8, wherein PMOS transistors P7 and P8 are coupled to an external power supply node EXV (see Morishita, Figure 2 and column 9, lines 11-19). However, there is no mention in Morishita of a first switching circuit that cuts off an external power voltage applied to the comparator CMM of Morishita when a control signal is activated. In addition, there is no mention in Morishita of a second switching circuit that cuts off a ground voltage supplied to the the comparator CMM of Morishita when a control signal is activated. In addition, there is no mention in Morishita of a third switching circuit including a CMOS transmission gate which transmits a driving signal when a control signal is inactivated. In sum, there is no disclosure in Morishita of either a first switching circuit, a second switching circuit, or a third switching circuit, as claimed. Reconsideration of the rejections of claims 23 and dependent claims 25, 27-29, and 32 thereon is respectfully requested.

In addition, with regard to dependent claims 7-9, 14-16, 27-29, 30-32, close inspection of Morishita reveals that Morishita fails to teach or suggest an input signal that is generated using a fuse, as claimed in claims 7, 14, and 27. Further, Morishita fails to teach or suggest an input signal that is generated using an external pad, as claimed in claims 8, 15, and 28. Further, Morishita fails to teach or suggest an input signal being a mode setting signal comprising a plurality of mode setting bits, as claimed in claims 9, 16, and 29. Further, Morishita fails to teach or suggest a value represented by mode setting bits and a mode setting command being used by a control signal generating circuit to generate a control signal, the value of the mode

setting bits corresponding to a number of bits being processed by a semiconductor device, as claimed in claims 30-32. Reconsideration and removal of the rejections of dependent claims 7-9, 14-16, 27-29, 30-32 are respectfully requested.

Therefore, it is submitted that Morishita fails to teach the invention set forth in the amended claims. Reconsideration and removal of the rejections of claims 1-3, 7-12, 14-16, 23, 25, and 27-32 under 35 U.S.C. 102(b) based on Morishita are therefore respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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